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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/972,178	10/09/2001	Hanae Shimokawa	500.38665CX1	5052

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EXAMINER

ZIMMERMAN, JOHN J

ART UNIT

PAPER NUMBER

1775

DATE MAILED: 06/04/2002

7

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/972,178

Applicant(s)

SHIMOKAWA ET AL.

Examiner

John J. Zimmerman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 March 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14, 19-27 and 40-59 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14, 19-27 and 40-59 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/581,631.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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OFFICE ACTION

Amendments

1. This Office Action is in response to the Amendment received March 18, 2002. Claims 1-14, 19-27 and 40-59 are pending in this application.

Information Disclosure Statement

2. The Information Disclosure Statement received March 6, 2002 has been considered and a completed form PTO-1449 is enclosed with this Office Action.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

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4. Claims 1-14, 19-27 and 40-59 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 14-50 of copending Application No. 09/581,631. Although the conflicting claims are not identical, they are not patentably distinct from each other because the scope of the pending claims of this application and the scope of the claims of the copending application overlap. The claims of both applications are directed to the same invention of using a Sn-Bi alloy layer on electronic articles and the use of lead free solders on these layers. It is noted that the both pending applications contain claims that are specific to the same types of devices (e.g. semiconductor devices - see claims 36-50 of SN 09/581,631 and claims 1-14, 19-27, 40-42 and 58-59 of SN 09/972,178) and electronic devices having electrodes and circuit boards (e.g. see claims 14-35 of SN 09/581,631 and claims 43-59 of SN 09/972,178). There is no patentable distinction between the two sets of pending claims. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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6. Claims 1-14, 19-27 and 40-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanimoto (U.S. Patent 6,110,608).

7. Tanimoto discloses forming electronic lead materials with a first coating of Sn-Bi alloy and a second solder coating which may be a Sn-Bi-Ag alloy (e.g. see column 3, line 63 - column 4, line 62). Specific examples of the Sn-Bi and Sn-Bi-Ag materials can be found in the tables (e.g. see Example 33 in Table 3 for specific Sn-Bi-Ag composition considered part of Tanimoto's invention and also see Example 44 in Table 3 which shows that the use of dual Sn layers containing Bi is part of Tanimoto's invention). The electrodes of Tanimoto may be copper plated (e.g. see column 6, lines 33-44). Tanimoto even discloses Sn-10%Bi plated without an intermediate layer or a second plated layer in Comparative Example 5 of Table 3. Tanimoto may differ from the claims in that Tanimoto may not have an example in the tables with Sn-Bi next to Sn-Bi-Ag solder. However, Tanimoto is not required to have made specific examples of each of his embodiments and Tanimoto clearly describes the compositions and requirements of his layers (e.g. see column 3, line 63 - column 4, line 62) and clearly discloses that the combinations of these disclosed layers are considered his invention. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use all the embodiments disclosed by Tanimoto because Tanimoto discloses that combinations of his disclosed layers are his invention. In addition, Tanimoto may not disclose the use of various substrates (e.g. Fe-Ni alloy) or various types of leads (e.g. TSOP leads). However, the examiner takes Official Notice that Fe-Ni alloy is

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conventionally used in the art as an alternative to copper alloy leads for semiconductor devices and the examiner also takes Official Notice that thin small outline package devices (TSOP) are conventional chip packages in the art. These alternative use of Fe-Ni alloy leads and the conventional use of TSOP devices is so well known in the art that Official Notice can be taken on these issues. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Fe-Ni alloys for the leads of Tanimoto because Fe-Ni alloys are understood in the art to be obvious alternatives to copper alloys for leads when thermal expansion issues, strength and expense are issues. In addition, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the compositions of the reference for TSOP devices because Tanimoto clearly discloses the use for analogous devices and it would be understood that leads of TSOP devices would benefit from the same coating compositions.

Response to Arguments

8. Applicant's arguments filed March 18, 2002 have been fully considered but they are not persuasive with regards to the remaining rejections.

9. Regarding the provisional rejection of claims 1-14, 19-27 and 40-59 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 14-50 of copending Application No. 09/581,631, applicant argues that the two sets of claims are patentably

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distinct. The examiner notes, however, that the claims of both applications are directed to the same invention of using a Sn-Bi alloy layer on electronic articles and the use of lead free solders on these layers. It is noted that the both pending applications contain claims that are specific to the same types of devices (e.g. semiconductor devices - see claims 36-50 of SN 09/581,631 and claims 1-14, 19-27, 40-42 and 58-59 of SN 09/972,178) and electronic devices having electrodes and circuit boards (e.g. see claims 14-35 of SN 09/581,631 and claims 43-59 of SN 09/972,178) with the same compositions and layers. There is no patentable distinction between the two sets of pending claims.

10. Regarding the rejection of claims 1-14, 19-27 and 40-59 under 35 U.S.C. 103(a) as being unpatentable over Tanimoto (U.S. Patent 6,110,608), Tanimoto remains particularly relevant to the pending claims since Tanimoto discloses forming electronic lead materials with a first coating of Sn-Bi alloy (e.g. column 6, lines 1-6) and a second lower melting point solder coating which may be Sn-Bi-Ag alloy (e.g. see column 3, line 63 - column 4, line 62). Specific examples of the Sn-Bi and Sn-Bi-Ag materials can be found in the tables (e.g. see Example 33 in Table 3 for specific Sn-Bi-Ag composition considered part of Tanimoto's invention and also see Example 44 in Table 3 which shows that the use of dual Sn layers containing Bi is part of Tanimoto's invention). The first Sn-Bi layer in Example 44 contains 2% Bi and the second Sn-Bi layer melts at a lower temperature than the first layer and thus functions as a lead free solder. The electrical

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leads of Tanimoto would necessarily be connected to a second electrical component (e.g. a circuit board, a chip, etc. . .) for it to perform its function (e.g. see Figure 3).

11. Applicant's argues that Tanimoto leads the skilled artisan to use a higher bismuth content in the tin layer than that required by the pending claims. A review of Tanimoto, however, clearly shows that Tanimoto's discussion of tin alloys with a higher bismuth content concerns the lower melting point second layer that functions as the lead free solder. Applicant limits the bismuth content to 1-5 wt.%, but only for the layer directly on the electrode. Tanimoto's layer that is directly on the electrode is Tanimoto's first layer. Tanimoto clearly discussed that the melting point of the first layer should be higher than the second (solder) layer and gives an example of Sn containing 2% Bi to achieve the higher melting point in the first layer (e.g. see Example 44; discussion in column 13, lines 1-4). It is clear that Tanimoto is in possession of the concept of using lower bismuth content tin alloys for coating a first layer on electrodes and then overplating with a lead free solder layer that will be used to connect the electrode to a second electrical component (e.g. Figure 3).

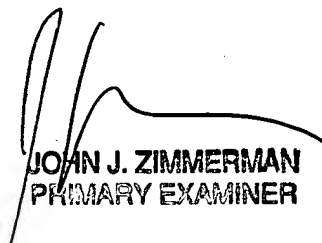
Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply

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is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Zimmerman whose telephone number is (703) 308-2512 and whose fax number is (703) 872-9310.



JOHN J. ZIMMERMAN
PRIMARY EXAMINER

jjz
May 31, 2002